# Lab 07

**Lab : 07**

**Name : MKSL Weerasiri**

**Registration Number : 220689N**

**Group No : 32**

# Introduction

## 1.1 Lab Task

In this lab, we are going to design and implement a 7–segment display. The 7 – Segment Display is a very basic display that has 7 segments to display a given value such as integers or some English letters. This lab is to connect it to our AU (Result of Lab 6) and display our AU results through it using a lookup table instead of using a logic function. Lookup table is a simple ROM, that is used to store and retrieve desired output without logic functions, just by looking at data in the memory.

## 1.2 Completed Table of Segments to Switch On

7 - Segment Display type in Basys3 board: common anode

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Output from RCA | | | | | Segments to Switch On | | | | | | |
| S3 | S2 | S1 | S0 | Hex. | A | B | C | D | E | F | G |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 3 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 4 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 5 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 7 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | A | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | B | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | C | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | E | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | F | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

# Lookup Table

## 2.1 Design Source File

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

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-- Create Date: 03/19/2024 01:09:33 PM

-- Design Name:

-- Module Name: LUT\_16\_7 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

USE IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity LUT\_16\_7 is

    Port ( address : in STD\_LOGIC\_VECTOR (3 downto 0);

           data : out STD\_LOGIC\_VECTOR (6 downto 0));

end LUT\_16\_7;

architecture Behavioral of LUT\_16\_7 is

TYPE rom\_type IS ARRAY (0 TO 15) OF STD\_LOGIC\_VECTOR (6 DOWNTO 0);

SIGNAL sevenSegment\_ROM : rom\_type := (

    "1000000",--0

    "1111001",--1

    "0100100",--2

    "0110000",--3

    "0011001",--4

    "0010010",--5

    "0000010",--6

    "1111000",--7

    "0000000",--8

    "0010000",--9

    "0001000",--A

    "0000011",--B

    "1000110",--C

    "0100001",--D

    "0000110",--E

    "0001110"--F

    );

begin

    data <= sevenSegment\_ROM (TO\_INTEGER(UNSIGNED(address)));

end Behavioral;

## 2.2 Elaborated Design Schematic

A screenshot of a computer

Description automatically generated

## 2.3 Simulation Source file

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

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-- Create Date: 03/19/2024 01:28:00 PM

-- Design Name:

-- Module Name: LUT\_16\_7\_Sim - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity LUT\_16\_7\_Sim is

--  Port ( );

end LUT\_16\_7\_Sim;

architecture Behavioral of LUT\_16\_7\_Sim is

COMPONENT LUT\_16\_7

    Port ( address : in STD\_LOGIC\_VECTOR (3 downto 0);

           data : out STD\_LOGIC\_VECTOR (6 downto 0));

END COMPONENT;

SIGNAL address : STD\_LOGIC\_VECTOR (3 DOWNTO 0);

SIGNAL data : STD\_LOGIC\_VECTOR (6 DOWNTO 0);

begin

    UUT : LUT\_16\_7

        PORT MAP(

            address => address,

            data => data

        );

    PROCESS

        BEGIN

            address <= "0000";WAIT FOR 100 NS;

            address <= "0110";WAIT FOR 100 NS;

            address <= "1010";WAIT FOR 100 NS;

            address <= "1111";WAIT FOR 100 NS;

    END PROCESS;

end Behavioral;

## 2.4 Timing Diagram

A screenshot of a computer

Description automatically generated

# 7 Segment Display

## 3.1 Design Source File

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

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-- Create Date: 03/19/2024 01:40:25 PM

-- Design Name:

-- Module Name: AU\_7\_Seg - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity AU\_7\_Seg is

    Port ( A : in STD\_LOGIC\_VECTOR (3 downto 0);

           Clk : in STD\_LOGIC;

           RegSel : in STD\_LOGIC;

           S\_LED : out STD\_LOGIC\_VECTOR (3 downto 0);

           S\_7Seg : out STD\_LOGIC\_VECTOR (6 downto 0);

           Carry : out STD\_LOGIC;

           Zero : out STD\_LOGIC);

end AU\_7\_Seg;

architecture Behavioral of AU\_7\_Seg is

COMPONENT AU

    Port ( A : in STD\_LOGIC\_VECTOR (3 downto 0);

           RegSel : in STD\_LOGIC;

           Clk : in STD\_LOGIC;

           S : out STD\_LOGIC\_VECTOR (3 downto 0);

           Zero : out STD\_LOGIC;

           Carry : out STD\_LOGIC);

END COMPONENT;

COMPONENT LUT\_16\_7

    Port ( address : in STD\_LOGIC\_VECTOR (3 downto 0);

           data : out STD\_LOGIC\_VECTOR (6 downto 0));

END COMPONENT;

SIGNAL S\_adder : STD\_LOGIC\_VECTOR (3 DOWNTO 0);

begin

    AU\_0 : AU

        PORT MAP(

            A => A,

            RegSel => RegSel,

            Clk => Clk,

            S => S\_adder,

            Carry => Carry,

            Zero => Zero

        );

    LUT\_16\_7\_0 : LUT\_16\_7

        PORT MAP(

            address => S\_adder,

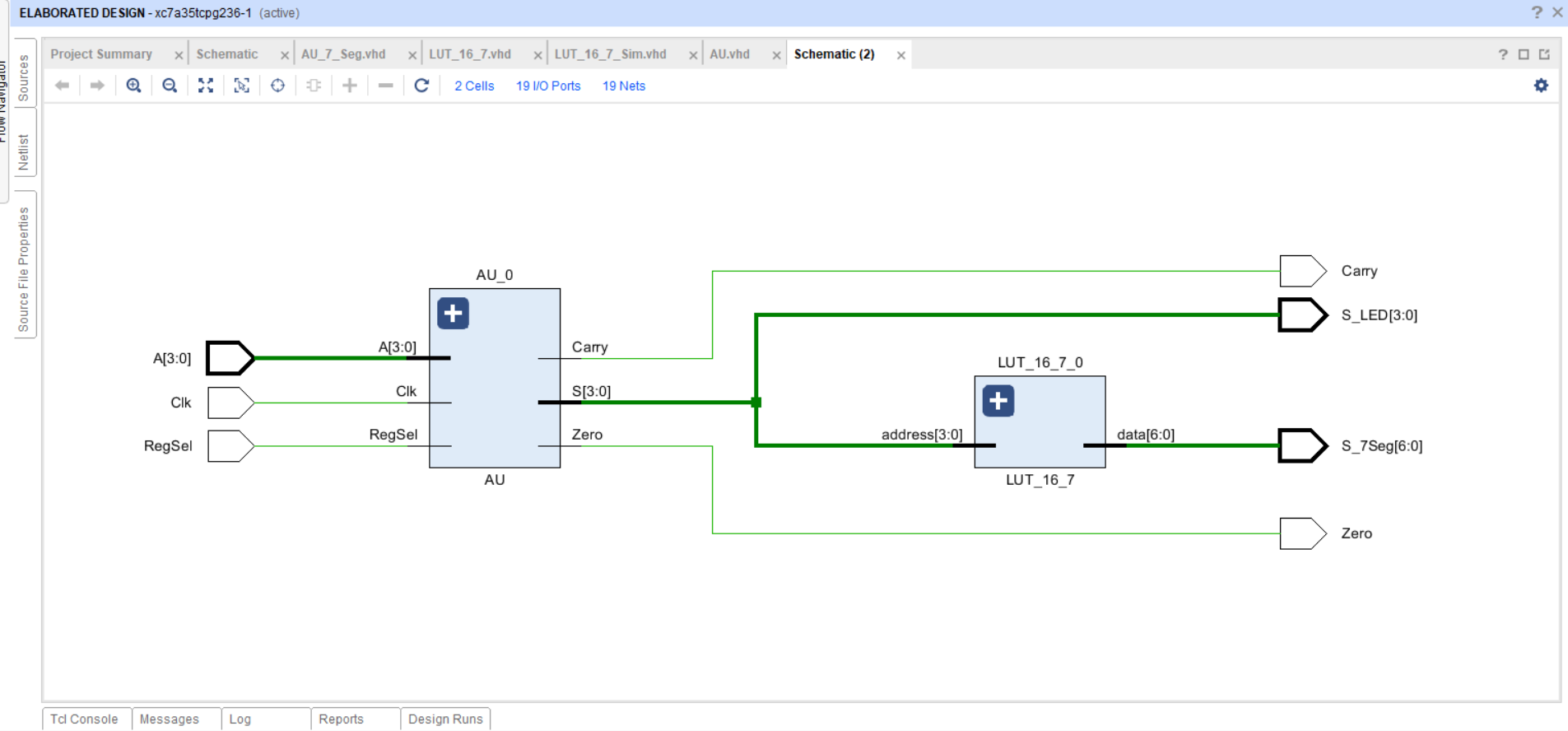
            data => S\_7Seg

        );

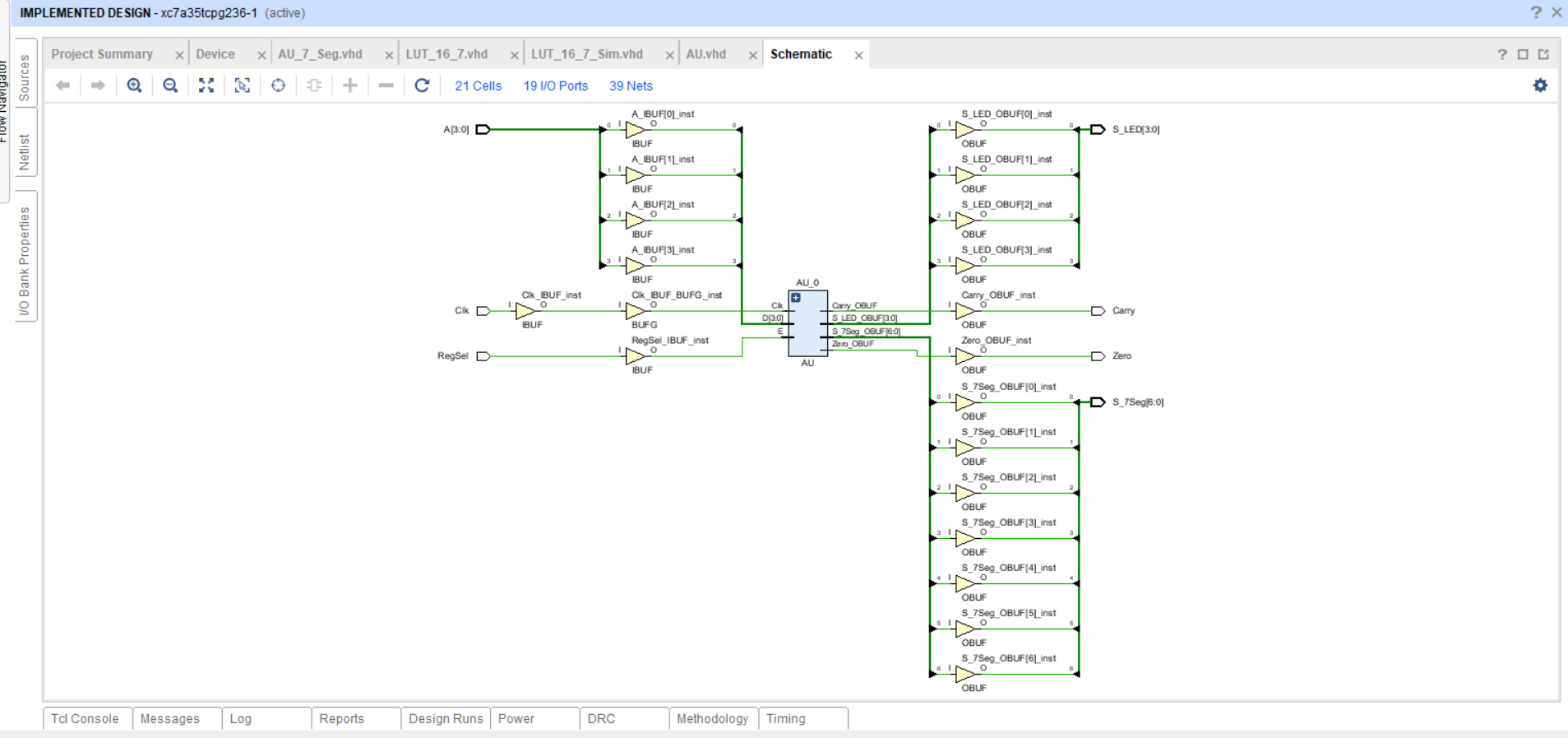
    S\_LED <= S\_adder;

end Behavioral;

## 3.2 Elaborated Design Schematic



## 3.3 Implemented Design Schematic



A screenshot of a computer

Description automatically generated

## 3.4 Constraints File

## Clock signal

set\_property PACKAGE\_PIN W5 [get\_ports Clk]

    set\_property IOSTANDARD LVCMOS33 [get\_ports Clk]

    create\_clock -add -name sys\_clk\_pin -period 10.00 -waveform {0 5} [get\_ports Clk]

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {A[0]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {A[0]}]

set\_property PACKAGE\_PIN V16 [get\_ports {A[1]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {A[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {A[2]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {A[2]}]

set\_property PACKAGE\_PIN W17 [get\_ports {A[3]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {A[3]}]

set\_property PACKAGE\_PIN R2 [get\_ports {RegSel}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {RegSel}]

## LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {S\_LED[0]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_LED[0]}]

set\_property PACKAGE\_PIN E19 [get\_ports {S\_LED[1]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_LED[1]}]

set\_property PACKAGE\_PIN U19 [get\_ports {S\_LED[2]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_LED[2]}]

set\_property PACKAGE\_PIN V19 [get\_ports {S\_LED[3]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_LED[3]}]

set\_property PACKAGE\_PIN P1 [get\_ports {Carry}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {Carry}]

set\_property PACKAGE\_PIN L1 [get\_ports {Zero}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {Zero}]

##7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {S\_7Seg[0]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_7Seg[0]}]

set\_property PACKAGE\_PIN W6 [get\_ports {S\_7Seg[1]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_7Seg[1]}]

set\_property PACKAGE\_PIN U8 [get\_ports {S\_7Seg[2]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_7Seg[2]}]

set\_property PACKAGE\_PIN V8 [get\_ports {S\_7Seg[3]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_7Seg[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {S\_7Seg[4]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_7Seg[4]}]

set\_property PACKAGE\_PIN V5 [get\_ports {S\_7Seg[5]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_7Seg[5]}]

set\_property PACKAGE\_PIN U7 [get\_ports {S\_7Seg[6]}]

    set\_property IOSTANDARD LVCMOS33 [get\_ports {S\_7Seg[6]}]

# Conclusion

In this lab, we have designed and implemented a simple display called a 7-segment display and checked it using our AU. And, to do that we have implemented a simple ROM to map our AU’s outputs to 7-segment display inputs.